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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,775	03/05/2002	Bruce E. Lavigne	100202224-1	8969

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EXAMINER	
WONG, WARNER	
ART UNIT	**PAPER NUMBER**
2668	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,775	LAVIGNE ET AL.	
	Examiner	Art Unit	
	Warner Wong	2668	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6-9,11,13-25 and 27-30* is/are rejected.

7)☒ Claim(s) *3,5,10,12 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. The following claims are objected to because of the following informalities:

Claim 16, line 3: The limitation "a memory request" appears to be referring to the same limitation in claim 15, line 16. It should be changed to "the memory request",

Claim 17, lines 2-3: The limitation "said packet" appearing as 2 instances in the claim is further described to be "at the head of said queue". Such description is contradictory to the referencing limitation "a packet which is not at a head of said queue" described in claim 15, line 17.

Claim 18, lines 2-3: The description "at said second packet processor" is redundant and may cause confusion. It should be removed.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-2, 4, 6, 8-9, 11, 13, 23-25 and 27-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Zuravleff (5,812,799).

Regarding claim 1, Zuravleff describes a method of speculatively issuing memory requests while maintaining a specified packet order comprising:

receiving a first, then a second incoming packet for forwarding (fig. 3a, "A1 request" and "A2 request" and fig. 5, #114, where I/O requests are queued in order of the request accordingly and that each request comprises the data [packet], fig. 6, & col. 7, lines 19-20);

sending a first memory request corresponding to said first packet (fig. 3a, "A1 request");

sending a second memory request corresponding to said second packet prior to receiving a first memory reply corresponding to said first memory request (fig. 3a "A2 request");

forwarding said first packet prior to forwarding said second packet (fig. 3a upon receiving "A1" reply" which indicates peripheral ready [fig., 11, #S40], the first packet is issued [fig. 11, #S60, fig. 6, #206 & col. 11, lines 3-5]; likewise for "A2 reply" for issuance of second packet);

Regarding claim 8, Zuravleff describes a network method comprising:

receiving a first anda second incoming packet for forwarding (fig. 3a, "A1 request" and "A2 request" and fig. 5, #114, where each request comprises the data [packet], fig. 6, & col. 7, lines 19-20);

sending a first memory request corresponding to said first packet (fig. 3a, "A1 request");

sending a second memory request corresponding to said second packet prior to forwarding said first packet (fig. 3a "A2 request" sent before receiving "A1" reply" which

indicates peripheral ready [fig., 11, #S40] and the first packet is then issued [fig. 11, #S60, fig. 6, #206 & col. 11, lines 3-5);

Regarding claim 23, Zuravleff describes a network device comprising:

Means to receiving a first, then a second incoming packet for forwarding (fig. 3a, "A1 request" and "A2 request" and fig. 5, #114, where I/O requests are queued in order of the request accordingly and that each request comprises the data [packet], fig. 6, & col. 7, lines 19-20);

sending a second memory request corresponding to said second packet prior to forwarding said first packet (fig. 3a "A2 request" sent before receiving "A1" reply" which indicates peripheral ready [fig., 11, #S40] and the first packet is then issued [fig. 11, #S60, fig. 6, #206 & col. 11, lines 3-5);

Regarding claim 24, Zuravleff further describes that the memory request of the first and second packets are maintained in a transfer order fig. 5, #114, where I/O requests are queued in order of the request accordingly and that each request comprises the data [packet], fig. 6, & col. 7, lines 19-20).

Regarding claims 2, 9 and 25, Zuravleff further describes that the first packet and said second packet are maintained in a transfer order queue (fig. 5, #114, where I/O requests are queued in order of the request accordingly and that each request comprises the data [packet], fig. 6, & col. 7, lines 19-20).

Regarding claim 4, 11 and 27, Zuravleff further describes that the first memory request is to request I/O resources to forward said first packet (col. 3, lines 61-67).

Regarding claim 6, 13 and 28, Zuravleff further describes receiving a first memory reply prior to forwarding said first packet (fig. 11, step S40 & S60, where the buffer issues memory transaction request (fig. 6, which includes the data packet) only after the peripheral is ready via a reply command, fig. 3a).

Regarding claim 29, Zuravleff describes all limitations set forth in claim 28. Zuravleff further describes accepting a memory reply prompts the process to execute and transfer the packet (assign network resource) (fig. 11, step S40 & S60, where the buffer issues memory transaction request (fig. 6, which includes the data packet) only after the peripheral is ready via a reply command, fig. 3a).

2. **Claims 7**, **14 and 30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuravleff as applied to claims 1, 8 and 23 above respectively, and further in view of Wakerly (5,875,466).

Zuravleff lacks what Wakerly describes: the first packet comprises an internet protocol (IP) packet for the purpose of abiding to the well-known IP protocol standard suitable to be used in existing Ethernet and FDDI networks.

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to describe received packets as IP packets. The motivation is that packets abiding to the well-known IP protocol standard are suitable to be used in existing Ethernet and FDDI networks (Wakerly , col. 14, lines 63-65).

3. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khacherian (6,542,507) in view of Zuravleff.

Regarding claim 15, Khacherian describes a switching (networking) device comprising:

an input port with controller (first packet processor) comprising:

an input interface having a port to accept incoming packets (fig. 3, #310);

an input memory coupled to said input interface for temporarily storing said packets in a queue arranged by a receiving order (col. 3, lines 64-67);

An output port with controller (second packet processor) comprising:

an output interface having a port to send said packets out of said networking device (fig. 3, #320);

an output memory coupled to said output interface for temporary storing said packets (fig. 3, #322);

a switching fabric coupled to said first packet processor and said second packet processor for conveying information between said first packet processor and said second packet processor (fig. 3, #300);

said first packet processor also for sending memory request (fig. #314, request to release);

In view of claim 15, Khacherian lacks what Zuravleff describes:

sending pipelined memory requests (request corresponding to a packet which is not at a head of said input queue) (fig. 3a, "A2 request"; fig. 5, #114, where requests to

forward the data to I/O are queued) for the purpose of allowing a high rate of transfer to memory and I/O devices for tasks which have real-time requirements.

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to incorporate the pipelined (memory) request approach of Zuravleff to the transfer methodology of the device of Khacherian. The motivation is that it allows a high rate of transfer to memory and I/O devices for tasks which have real-time requirements (Zuravleff, col. 3, lines 43-45).

Regarding claim 16, Khacherian further describes that the input port with controller (first packet processor) also receives a Grant-to-Release (memory) reply message from the output port controller (second packet processor) corresponding to a Request-to-Release (memory request) for a packet (fig. 3, #414, 324; col. 4, lines 13-21).

Regarding claim 17, Khacherian further describes that the input port with controller (first packet processor) sends packets to the output port with controller (second packet processor) if the packet is at the head of said queue (fig. 3 & col. 5, lines 40-43, where packets in queues of source input port #310 are switched to destination output port #320 via the fabric #300).

Regarding claim 18, Khacherian further describes that the output port with controller (second packet processor) receives the packet (fig. 3 & col. 5, lines 40-43, where packets in queues of source input port #310 are switched to destination output port #320 via the fabric #300).

Regarding claim 19, Khacherian further describes that the output port with controller (second packet processor) sends the packet out of the switching/networking device (fig. 3, "physical output" from #320).

Regarding claim 20, Khacherian further describes that there are a plurality of input/output ports with controllers (packet processors) in addition to the (first) input port and the (second) input port coupled to said switching fabric (fig. 2 & col. 3, lines 57-60, where plurality of input/output ports, each with a controller).

4. **Claim 21** is rejected under 35 U.S.C. 103(a) as being unpatentable over Khacherian in view of Zuravleff as applied to claim 15 above, and further in view of Hanaoka (6,584,103)

In view of claim 21, Khacherian and Zuravleff combined lack what Hanaoka describes: the memory request comprises a first portion to indicate that said packet is not at a head of said queue (fig. 3 & 4, "t-labels", & col. 2, lines 60-67, where t-label indicates the sequence of packet request, i.e. whether or not the data is at the head of the originating device/queue requesting the transfer of such data) for the purpose of distinguishing a plurality of packets having the identical source and the identical destination.

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to incorporate the use of labels to the headers of packet (memory) request as in Hanaoka for the requests used in the combined device of

Khacherian and Zuravleff. The motivation is that it distinguishes a plurality of packets having the identical source and the identical destination.

5. **Claim 22** is rejected under 35 U.S.C. 103(a) as being unpatentable over Khacherian in view of Zuravleff as applied to claim 15 above, and further in view of Wakerly.

In view of claim 22, Khacherian and Zuravleff combined lack what Wakerly describes: the packet is an internet protocol (IP) packet for the purpose of abiding to the well-known IP protocol standard suitable to be used in existing Ethernet and FDDI networks.

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to describe the packets handled by the combined device of Khacherian and Zuravleff as IP packets as in Wakerly. The motivation is that packets abiding to the well-known IP protocol standard are suitable to be used in existing Ethernet and FDDI networks (Wakerly , col. 14, lines 63-65).

Allowable Subject Matter

6. Claims 3, 5, 10, 12, 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jeddeloh (6,295,592), Heddes (5,432,908), Tsai (6,718,400), Divivier (5,752,269), Kessler (6,754,739), Kootstra (2003/0188088), Pong (6,728,843) and Garde (5,787,488).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Warner Wong whose telephone number is 571-272-8197. The examiner can normally be reached on 5:30AM - 2:00PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Warner Wong
Examiner
Art Unit 2668

WW

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